



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1480
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,010	08/22/2003	Timothy E. Hoglund	03-0084	8967

7590 04/16/2007
LSI Logic Corporation
Corporate Legal Department, M/S D-106
Intellectual Property Services Group
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER

GANDHI, DIPAKKUMAR B

ART UNIT	PAPER NUMBER
----------	--------------

2117

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/646,010

Applicant(s)

HOGLUND ET AL.

Examiner

Dipakkumar Gandhi

Art Unit

2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) 7 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 8-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

1. Applicants' request for reconsideration filed on 01/19/2007 has been reviewed.
2. Amendment including amended claims filed on 01/19/2007 has been entered.
3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2, 5, 6, 8, 9, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nance et al. (US 5,715,197) in view of Conner (US 4,450,560) and Tovey (US 6,643,673 B1).

As per claim 1, Nance et al. teach a method for observing the state of internal signals, comprising: receiving specific signals by a plurality of multiplexers in at least one module; combining by the plurality of multiplexers, signals received to create a plurality of signals; receiving, by mapping logic, one of said plurality of signals from each one of said plurality of multiplexers (fig. 1, 2, col. 3, lines 33-39, col. 4, lines 36-38, col. 5, line 55 to col. 6, line 32, col. 7, lines 45-46, Nance et al.).

However Nance et al. do not explicitly teach the specific use of chip testing and test signal groups.

Conner in an analogous art teaches that the invention features in one aspect apparatus for testing LSI and memory devices by injecting test signals (col. 1, lines 31-33, Conner). Conner also teaches a group

Art Unit: 2117

sequence generator for causing the format and timing generator to provide updated format and timing information corresponding to groups of the test signals and the standards for testing the memory devices (col. 1, lines 55-59, Conner).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nance et al.'s patent with the teachings of Conner by including an additional step of using the test signal groups.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the test signal groups would provide the opportunity to simultaneously analyze the test signals.

Nance et al. also do not explicitly teach the specific use of mapping, by said mapping logic, one of said plurality of signals to at least two of said plurality of outputs of said mapping logic concurrently to output as two different signals.

However Tovey in an analogous art teach that FIG. 4 illustrates...outputs an 8 bit value (fig. 4, col. 5, lines 31-44, Tovey).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nance et al.'s patent with the teachings of Tovey by including an additional step of using mapping, by said mapping logic, one of said plurality of signals to at least two of said plurality of outputs of said mapping logic concurrently to output as two different signals.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to receive same input signal as two different output signals.

- As per claim 2, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the method wherein the at least one module includes a plurality of modules (fig. 1, col. 3, lines 33-35, Nance et al.).

- As per claim 5, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the method further comprising: said mapping logic including a plurality of mapping multiplexers; each one of said plurality of mapping multiplexers receiving said plurality of signals; each

Art Unit: 2117

one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and each one of said plurality of mapping multiplexers selecting one of said plurality of signals to output (fig. 1, col. 4, lines 36-41, Nance et al.).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

- As per claim 6, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the method wherein said mapping logic is byte lane mapping logic (col. 2, lines 15-17, Nance et al.).

- As per claim 8, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach a system for observing the state of internal signals, comprising: means for receiving specific signals by a plurality of multiplexers in at least one module; the plurality of multiplexers combining the specific signals received to create a plurality of signals; mapping logic for receiving one of said plurality of signals from each one of said plurality of multiplexers (fig. 1, 2, col. 3, lines 33-39, col. 4, lines 36-38, col. 5, line 55 to col. 6, line 32, col. 7, lines 45-46, Nance et al.).

Conner teaches chip testing and test signal groups (col. 1, lines 31-33, col. 1, lines 55-59, Conner).

Tovey teaches mapping logic, mapping one of said plurality of signals to at least two of said plurality of outputs of said mapping logic concurrently to output as two different signals (fig. 4, col. 5, lines 31-44, Tovey).

- As per claim 9, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the system wherein the at least one module includes a plurality of modules (fig. 1, col. 3, lines 33-35, Nance et al.).

- As per claim 12, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the system further comprising: said mapping logic including a plurality of mapping multiplexers; each one of said plurality of mapping multiplexers receiving said plurality of signals; each one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and each one of said plurality of mapping multiplexers selecting one of said plurality of signals to output (fig. 1, col. 4, lines 36-41, Nance et al.).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

Art Unit: 2117

- As per claim 13, Nance et al., Conner and Tovey teach the additional limitations.

Nance et al. teach the system wherein the mapping logic is byte lane mapping logic (col. 2, lines 15-17, Nance et al.).

7. Claims 3, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nance et al. (US 5,715,197), Conner (US 4,450,560) and Tovey (US 6,643,673 B1) as applied to claim 2 and 9 above, and further in view of Swart (US 5,389,885).

As per claim 3, Nance et al., Conner and Tovey substantially teach the claimed invention described in claim 2 (as rejected above).

However Nance et al., Conner and Tovey do not explicitly teach the specific use of the method, further comprising: concurrently observing test signals for a plurality of modules.

Swart in an analogous art teaches that electrical test signals...under test (col. 8, line 65 to col. 9, line 2, Swart).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nance et al.'s patent with the teachings of Swart by including an additional step of using the method, further comprising: concurrently observing test signals for a plurality of modules.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, further comprising: concurrently observing test signals for a plurality of modules would provide the opportunity to compare test signals output from different modules and analyze the signals.

- As per claim 10, Nance et al., Conner, Tovey and Swart teach the additional limitations.

Swart teaches the system, further comprising: concurrently observing test signals for a plurality of modules (col. 8, line 65 to col. 9, line 2, Swart).

8. Claims 4, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nance et al. (US 5,715,197), Conner (US 4,450,560), Tovey (US 6,643,673 B1) and Swart (US 5,389,885) as applied to claims 3 and 10 above, and further in view of Moore et al. (US 5,604,432).

As per claim 4, Nance et al., Conner, Tovey and Swart substantially teach the claimed invention described in claim 3 (as rejected above).

Art Unit: 2117

However Nance et al., Conner, Tovey and Swart do not explicitly teach the specific use of the method, wherein the plurality of modules includes identical modules.

Moore et al. in an analogous art teach that it is desirable to be able to use the same test vectors for identical modules (col. 4, lines 43-44, Moore et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nance et al.'s patent with the teachings of Moore et al. by including an additional step of using the method, wherein the plurality of modules includes identical modules.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, wherein the plurality of modules includes identical modules would provide the opportunity to compare the test signal output simultaneously from the identical modules.

- As per claim 11, Nance et al., Conner, Tovey, Swart and Moore et al. teach the additional limitations.

Moore et al. teach the system wherein the plurality of modules includes identical modules (col. 4, lines 43-44, Moore et al.).

9. Claims 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nance et al. (US 5,715,197), Conner (US 4,450,560) and Tovey (US 6,643,673 B1) as applied to claim 1, 8 above, and further in view of Wittig et al. (US 6,118,300).

As per claim 14, Nance et al., Conner and Tovey substantially teach the claimed invention described in claim 1 (as rejected above). Conner also teaches test signal groups (col. 1, lines 55-59, Conner).

However Nance et al., Conner and Tovey do not explicitly teach the specific use of the method further comprising: mapping, by said mapping logic, a first one of said plurality of signals, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first output; mapping, by said mapping logic, a second one of said plurality of signals, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second output; and said first one of said plurality of signals and said second one of said plurality of signals being a same signal type of signal.

Art Unit: 2117

Wittig et al. in an analogous art teach that FIG. 2A illustrates a wide multiplexer...output port OUT (fig. 2B, col. 5, lines 59-65, Wittig et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nance et al.'s patent with the teachings of Wittig et al. by including an additional step of using the method further comprising: mapping, by said mapping logic, a first one of said plurality of signals, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first output; mapping, by said mapping logic, a second one of said plurality of signals, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second output; and said first one of said plurality of signals and said second one of said plurality of signals being a same signal type of signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to output desired test signals using a mapping logic.

- As per claim 15, Nance et al., Conner, Tovey and Wittig et al. teach the additional limitations.

Wittig et al. teach the system further comprising: said mapping logic mapping a first one of said plurality of signals, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first output group; said mapping logic mapping a second one of said plurality of signals, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second output group; and said first one of said plurality of signal groups and said second one of said plurality of signal groups being a same signal type of a signal (fig. 2B, col. 5, lines 59-65, Wittig et al.).

Conner teaches test signal groups (col. 1, lines 55-59, Conner).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2117

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2117

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Dipakkumar Gandhi
Patent Examiner



GUY LAMARRE
PRIMARY EXAMINER